SECTION OF ELECTRICAL ENGINEERING

EPFL STI – SEL
ELG
Station nº 11
CH-1015 Lausanne

Téléphone : +4121 693 1346
Fax :
E-mail : alexandre.levisse@epfl.ch
Site web : epfl.ch

ADVANCED VLSI DESIGN

Guidelines for the final presentation content
GRADED

In the Final Presentation, you are expected to summarize the content of the MidTerm presentation (i.e., the design itself and rapidly the floorplan, as adapted to the final design), as well as explain all the items mentioned below.

1. The screenshots, x-y dimensions and areas of the layouts:
    a. Layout of the entire Accumulator block.
    b. Layouts of selected interesting individual blocks (at least 2). For example:
        - The flip flop (FF)
        - Carry select adder (CSA)
        - propagate-generate producer and carry-merge block (highlighting the sub-blocks

In your design, there will be 128 FFs and 15/16 CSAs; however, in the presentation you need to show only one FF layout and only one CSA layout. Same for the propagate-generate producer and carrymerge block. While presenting the layouts, please indicate the dimensions in the x and y directions. You can do this by using the ruler property of Cadence. Moreover, you should point out the used metal layers for each of the layouts.

2. Discuss the final layout (equivalent to final floorplan which should correspond to the layout) and important items such as clock and power distribution, the structure and strategy why it is as it is. Discuss how it is composed (vertical vs horizontal slices, what was is the thinking behind the structure you have chosen)
3. Critical Path Simulations:
    a. You should present 2 simulation results which are:
        - Schematic (without any extraction and without any additional cap instantiation)
        - Coupled C extracted

Present the analysis and delay of the critical path as in midterm presentation. You can refer to point 4 of the previous document containing the content of the midterm presentation. Clearly indicate
the propagation of the signals through your critical path. Plot all the signals on the critical path of

your circuit (from the output of the register to the input of the register) when the critical path vectors are applied. Clearly indicate the name of the first and the last signal between the registers. Plot all the signals on the same waveform window on top of each other for 2 different cases. At the end, show 2 different screenshots for 2 different simulation cases.
Important Note: In order to observe the signal of a specific node in the post layout simulations, you need to access that signal in your extracted view. For that you need to save the waveforms.

You could refer to the following link :
https://tclgit.epfl.ch/lfschmid/vlsi2/blob/master/PROBENETS.md

4. In your presentation you should state the worst case register to register delay of your design. And based on this value, you need to calculate the maximum clock frequency of your implementation. These two measurements are important specifications of this project. Also provide an analysis of the clock distribution: show some important clock leaf nodes and mention the clock skew you observe.
5. Quality of the Presentation:

Please note that this presentation is equal to the final exam of this course. Therefore, pay attention to the quality of your slides and your presentation. In order to have a good presentation, do not hesitate to use bullets, figures, tables, etc. wherever they are useful. Avoid writing long sentences onto the slides.

6. Provide us the library of your design in moodle, as a tar file. The procedure is described on moodle.